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10/587,608	07/27/2006	Francesco Pessolano	NL04 0078 US1	9958

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EXAMINER	
PATHAK, SUDHANSHU C	

ART UNIT	PAPER NUMBER
2611	

NOTIFICATION DATE	DELIVERY MODE
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

ip.department.us@nxp.com

Response to Arguments

1. Applicant's arguments filed in amendment dated 07/14/2009 have been fully considered but they are not persuasive. **The office action (OA) below further clarifies the examiner's interpretation of the Liu et al. (6,219,797) reference**.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

   A person shall be entitled to a patent unless –

   (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-2, 9, 14, 16-17 (device) & 15, 18 (method) are rejected under 35 U.S.C. 102(b) as being anticipated by Liu et al. (6,219,797).

In regards to Claims 1-2, 9, 14-18, Liu discloses an electronic device (method) for generating a clock signal for an integrated circuit (Fig. 5), the device comprising: at least two clock generation elements configured to generate a single clock signal at a clock output in response to an input signal and to operate in a mutually exclusive manner, the outputs of said clock generation elements being selectively connectable to said clock output the device (Fig. 5, element 74, 86, 78) {Interpretation: The reference discloses the division elements generating multiple clocks and further the "Mux" selects a single clock from the multiple options}: means for receiving a data pattern representative of a sequence of frequencies at which said clock signal is required to be generated (Fig. 5, elements “CD0” & “CD1”) {Interpretation: The reference discloses a plurality of bits (patterns) so as to select

different frequency signals and the selection of a certain bit (pattern) selects a certain frequency clock. This interpretation is consistent with the instant application specification as recited on Page 5, lines 28-29 which states **"The device comprises an arbiter 22 for receiving requests to change the frequency of the clock signal…", thus each bit combination of "CD0" & "CD1" is interpreted as a request. Furthermore, the claim does not recite receiving a single pattern representing all the plurality of frequencies i.e. a single pattern for all the switching frequencies**}; means for causing a clock generation element other than the clock generation element generating the clock signal at the immediately previous frequency in said sequence to generate a clock signal at said next frequency and means for causing the clock signal at the immediately previous frequency in said sequence to be disconnected from said clock output and further means for causing the clock signal at the next frequency in said sequence to be connected to said clock output **(Fig. 5, element 74, 78, 86) {Interpretation the reference discloses plurality of different clock generation elements i.e. div. "1024", "64" wherein the clock generation elements are different and depending on the pattern the other elements are disconnected or connected depending on the desired clock frequency**}; wherein the clock generation element being caused to generate a clock signal at each frequency in said sequence is independent of the value of said frequency (Fig. 5, element 70, 72, 74, 78, 86 & Column 12, lines 53-67) {Interpretation: The reference discloses plurality of clock source elements i.e. crystal

and ring oscillator which are separate and independent and the clock generation elements can generate frequencies with either source}.

Conclusion

4. Any inquiry concerning this communication or earlier communications from the examiner should be directed to SUDHANSHU C. PATHAK whose telephone number is (571)272-5509. The examiner can normally be reached on 9am-5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chieh M. Fan can be reached on 571-272-3042. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Sudhanshu C Pathak/
Primary Examiner, Art Unit 2611